

Unit I : Design with HDL

Assignment No.1

Write any five

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|----|---|-----|
| Q1 | Explain any two modelling styles in VHDL. | CO1 |
| Q2 | Write VHDL code and test bench for D flip flop | CO1 |
| Q3 | Explain signal and variable differences in VHDL. | CO1 |
| Q4 | Explain function and procedure with example. | CO1 |
| Q5 | Explain any two concurrent statements in VHDL with syntax. | CO1 |
| Q6 | Design bit shift Register using VHDL programming. | CO1 |
| | Also write Test bench for the same. | |
| Q7 | Explain different types of wait statements used in VHDL, with suitable example. | CO1 |

Unit II : Digital design and Issues

Assignment No.2

Write any five

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| Q1 | What is supply and ground bounce? What are remedies to it? | CO2 |
| Q2 | What is the need of clock distribution? Explain techniques of clock distribution. | CO2 |
| Q3 | Draw FSM diagram and write VHDL code for 100 Moore sequence detector. | CO2 |
| Q4 | Draw CPLD architecture in detail. Explain in brief. | CO2 |
| Q5 | Give typical features and specifications of FGPA. | CO2 |
| Q6 | What is clock skew? What are techniques to minimize? | CO2 |
| Q7 | Why should supply and ground bounce be taken care? How are these minimized? | CO2 |
| Q8 | Explain signal integrity issues involved in VLSI design. | CO2 |

Unit III: PLD Architecture and Applications

Assignment No.3

Write any five

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| Q1 | Draw CPLD XC9500 series architecture and explain in details. | CO3 |
| Q2 | Describe the PLD design flow. What are the limitations of PLD architecture. | CO3 |
| Q3 | Draw and explain the detail architecture of FPGA. | CO3 |
| Q4 | Compare CPLD and FPGA. What is need of CPLD? | CO3 |
| Q5 | Draw and explain the following for FPGA | CO3 |
| | i. Logic cell | |
| | ii. CLB | |
| | iii. Programmable switch matrix | |
| | iv. I/O block | |
| Q6 | With the help of suitable schematics, compare PROM, PLA and PAL architectures. | CO3 |
| Q7 | Explain with suitable diagram SRAM and anti-fuse programming techniques used in FPGA. | CO3 |
| Q8 | What is a role of CPLD and FPGA in embedded system developments? | CO3 |

Unit IV: Digital CMOS Circuits

Assignment No.4

Write any five

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| Q1 | Explain the following: | CO4 |
| | i) Body Effect | |
| | ii) Hot electron Effect | |
| Q2 | Derive the static and dynamic power dissipation in CMOS. | CO4 |
| Q3 | Explain the working of transmission gate and implement a circuit of 2:1 multiplexer using transmission gate. | CO4 |
| Q4 | Draw NAND, NOR, AND, OR, EX-OR gates using CMOS. | |
| Q5 | Draw and Explain RC Delay Model for NMOS and PMOS transistor.
Give example. | CO4 |
| Q6 | Design CMOS logic for $Y = ABC + D$.
Calculate W/L ratio for NMOS and PMOS are needed on chip. | CO4 |
| Q7 | Define scaling and explain any one type of scaling. | CO4 |

Unit V: Application Specific Integrated Circuit

Assignment No.5

Write any five

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|----|---|-----|
| Q1 | Which lambda rules are used for CMOS layout? Give its significance | CO5 |
| Q2 | Explain Design issues like antenna effect and electro migration effect. | CO5 |
| Q3 | Draw stick diagram for CMOS inverter, NAND, NOR gate. | CO5 |
| Q4 | Explain in detail micron-based design rules. | CO5 |
| Q5 | Write in lambda rules with diagram. | CO5 |
| Q6 | Explain Parasitic extraction. Explain Crosstalk in detail. | CO5 |
| Q7 | Explain Static Timing Analysis. | CO5 |

Unit VI: Digital CMOS Circuits

Assignment No.6

Write any five

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|----|---|-----|
| Q1 | Compare data flow, behavioral and structural modeling. | CO6 |
| Q2 | Write code in VHDL for 4:1 multiplexer in three different modeling types. | CO6 |
| Q3 | Design CMOS logic for $Y = A + BC + DE$. Calculate the area in terms of W. | CO6 |
| Q4 | What are the effects of technology scaling on chip level design? | CO6 |
| Q5 | Describe the following:
a. BSDF
b. JTAG | CO6 |
| Q6 | Explain Stuck-at-0 and stuck-at-1 faults. | CO6 |
| Q7 | Write short notes on :
a. ASIC
b. ASIC design flow. | CO6 |